AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. ***(currently amended)*** A semiconductor packaging device comprising:

a carrier having at least a portion configured for containing a chip ~~cavity thereon~~;

at least a chip having a back surface and an active surface, and a sidewall connecting said back surface and said ~~active surface, wherein said chip is affixed to said cavity to expose said active surface, and said active surface has a plurality of first bonding pads~~ ,wherein said sidewall is affixed to said portion and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, ~~said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads and via said first insulating layer~~ wherein a plurality of first conductive holes in said first insulating layer are corresponding to said first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure ~~comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, and a second insulating layer and a plurality of exposed ball pads thereon, wherein said first plating through holes are electrically connected with said conductive layout lines, said second plating through holes, and said exposed ball pads~~ configured for providing electrical connection to said first conductive holes;

a second insulating layer affixed on one of said carrier and said multi-layer structure, wherein said second insulating layer has a plurality of second conductive holes electrically connected to said first conductive holes; and

a plurality of solder balls ~~affixed to said ball pads~~ on at least one of said carrier and said second insulating layer, wherein said solder balls electrically connected said second conductive holes.

2. *(currently amended)* The semiconductor packaging device of claim 1, wherein said carrier is further configured for providing electrical connection between said second conductive holes and said first conductive holes when said second insulating layer is affixed on said carrier ~~made of a material selected from groups of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above~~.

3. *(currently amended)* The semiconductor packaging device of claim [[1]]2, wherein said carrier has a plurality of third conductive holes therein ~~comprises a substrate with a circuit layer that said substrate is selected from the groups of ceramic substrate, an organic substrate, or combination of above~~.

4. *(currently amended)* The semiconductor packaging device of claim 1, wherein said back surface is affixed to said portion ~~ball pads are distributed at a location selected from the groups of above said chip, above surrounding of said chip, or combination of above~~.

5. *(currently amended)* The semiconductor packaging device of claim 4, wherein said portion comprises a cavity. ~~A semiconductor packaging device comprising:~~

~~a carrier having at least a slot via said carrier;~~

~~at least a chip having a back surface and an active surface, wherein said chip is affixed to said slot to expose said active surface, and said active surface has a plurality of first bonding pads;~~

~~a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads and via said first insulating layer;~~

~~a multi layer structure on said first insulating layer, said multi layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, and a second insulating layer and a plurality of exposed ball pads thereon, wherein said first plating through holes are electrically connected with said conductive layout lines, said second plating through holes, and said exposed ball pads; and~~

~~a plurality of solder balls affixed to said ball pads.~~

6. ***(currently amended)*** The semiconductor packaging device of claim [[5]]1, wherein said portion is a cavity ~~carrier is made of a material selected from groups of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above~~.

7. ***(currently amended)*** The semiconductor packaging device of claim [[5]]1, wherein said portion is a slot ~~carrier comprises a substrate with a circuit layer that said substrate is selected from the groups of ceramic substrate, an organic substrate, or combination of above~~.

8. ***(currently amended)*** The semiconductor packaging device, comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said back surface and said sidewall are affixed to said cavity and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer on said multi-layer structure, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads. ~~of claim 5, wherein said ball pads are distributed at a location selected from the groups of above said chip, above surrounding of said chip, or combination of above.~~

9. ***(currently amended)*** The semiconductor packaging device of claim 8, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above. ~~A semiconductor packaging device comprising:~~

~~a carrier having a circuit layout therein, a first surface with a plurality of ball pads, and a second surface with a cavity thereon and a plurality of first bonding pads;~~

~~at least a chip having a back surface and an active surface with a plurality of second bonding pads thereon, wherein said chip is affixed to said cavity to expose said active surface;~~

~~a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads, said second bonding pads, and said first plating through holes via said first insulating layer;~~

~~a multi-layer structure on said first insulating layer, said multi-layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, wherein said conductive layout lines, said second plating through holes are connected to said first plating through holes and electrically connected to said ball pads; and~~

~~a plurality of solder balls affixed to said ball pads.~~

10. ***(currently amended)*** The semiconductor packaging device of claim 8, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip. ~~The semiconductor packaging device of claim 9, wherein said carrier comprises a substrate selected from the groups of ceramic substrate, an organic substrate, or combination of above.~~

11. ***(currently amended)*** A semiconductor packaging device, comprising:

a carrier having at least a slot therein configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said sidewall is affixed to a sidewall of said slot and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer on said back surface and said carrier, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and a plurality of solder balls affixed to said ball pads. ~~A semiconductor packaging device comprising:~~

~~a carrier having a circuit layout therein, a first surface with a plurality of ball pads, and a second surface with a slot via said carrier and a plurality of first bonding pads;~~

~~at least a chip having a back surface and an active surface with a plurality of second bonding pads thereon, wherein said chip is affixed to said slot to expose said active surface on said second surface and expose said back surface on said first surface;~~

~~a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads, said second bonding pads, and said first plating through holes via said first insulating layer;~~

~~a multi layer structure on said first insulating layer, said multi layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, wherein said conductive layout lines, said second plating through holes are connected to said first plating through holes and electrically connected to said ball pads; and~~

~~a plurality of solder balls affixed to said ball pads.~~

12. ***(currently amended)*** The semiconductor packaging device of claim 11, wherein said carrier has a plurality of third conductive holes electrically connecting said second conductive holes and said ball pads. ~~The semiconductor packaging device of claim 11, wherein said carrier comprises a substrate selected from the groups of ceramic substrate, an organic substrate, or combination of above.~~

13. **(new)** The semiconductor packaging device of claim 11, wherein said solder balls are distributed around said chip.

14. **(new)** The semiconductor packaging device of claim 11, wherein said solder balls and said back surface are on a same side.

15. **(new)** A semiconductor packaging device, comprising:

a carrier having at least a cavity therein, said cavity configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said back surface and said sidewall are affixed to said cavity and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer, at a same side with said back surface, affixed to said carrier, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

16. **(new)** The semiconductor packaging device of claim 15, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.

17. **(new)** A semiconductor packaging device, comprising:

a carrier having at least a slot therein configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said sidewall affixes to said slot and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer affixed to multi-layer structure, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

18. **(new)** The semiconductor packaging device of claim 17, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

19. **(new)** The semiconductor packaging device of claim 17, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.